

Abstract of the Disclosure

A logic system for resolving port contentions associated with memory-access requests in data packet routing is provided. The logic
5 system comprises a determination logic for assessing and reporting port status of busy or not busy, a command mechanism for issuing commands contingent on determination results and a staged buffer memory for holding pending requests waiting for permission to access the memory. A single request at the head of the buffer memory is considered for port
10 access whereupon if a port is determined to be busy, the command logic issues appropriate commands to units responsible for downloading packets from the memory and for sending new memory-access requests.

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